CLAIMS

What is claimed is:

1. A method for identifying a sequence of best sampling positions for sampling a data signal having a data eye and a variable bit rate, from samples of the data signal generated using an oversampling clock having sampling positions, where the data eye has a center, said method including the steps of:

(a) generating, from the samples, relative phase data indicative of the phase of each of at least one of the sampling positions relative to the center of the data eye, for each of a number of tracking periods of the data signal; and

(b) determining from the relative phase data which of the sampling positions is best aligned with the center of the data eye during each of at least some of the tracking periods, thereby identifying the sequence of best sampling positions, wherein step (b) includes the steps of:

(c) applying a first low-pass filter to the relative phase data for at least one of the tracking periods in response to determining that the data signal's bit rate is in a first frequency range; and

(d) applying one of a second low-pass filter and no low-pass filter to the relative phase data for at least another one of the tracking periods in response to determining that the data signal's bit rate is in a second frequency range, where the second frequency range is different than the first frequency range and the second low-pass filter is different than the first low-pass filter.

2. The method of claim 1, wherein step (c) includes the steps of:

generating filtered data by applying the first low-pass filter to the relative phase data for a first sequence of the tracking periods; and

when one of the sampling positions has been identified as one of the best sampling positions, continuing to identify said one of the sampling positions as said one of the best sampling positions until the filtered data indicate that said one of the sampling positions has phase that leads the center of the data eye for N consecutive ones of the first sequence of the tracking periods, or lags the center of the data eye for N consecutive ones of the first sequence of the tracking periods.

3. The method of claim 2, wherein the second frequency range is lower than the first frequency range, and step (d) includes the steps of:

generating additional filtered data by applying the second low-pass filter to the relative phase data for a second sequence of the tracking periods; and

when one of the sampling positions has been identified as one of the best sampling positions, continuing to identify said one of the sampling positions as said one of the best sampling positions until the additional filtered data indicate that said one of the sampling positions has phase that leads the center of the data eye for M consecutive ones of the second sequence of the tracking periods, or lags the center of the data eye for M consecutive ones of the second sequence of the tracking periods, where $2 \leq M$, and $M < N$.

4. The method of claim 1, wherein the second frequency range is lower than the first frequency range, no low-pass filter is applied to the relative phase data during step (d), and step (d) includes the step of:

when one of the sampling positions has been identified as one of the best sampling positions, identifying another one of the sampling positions as the best sampling position if the relative phase data indicate that said one of the sampling positions has phase misaligned with the center of the data eye for one of the tracking periods.

5. The method of claim 1, also including the steps of:

generating a count indicative of the number of cycles of a data clock that occur during a predetermined number of cycles of a second clock having a fixed, predetermined frequency, where the data clock has frequency indicative of the data signal's bit rate; and

determining that the data signal's bit rate is in the first frequency range only if the count exceeds a predetermined threshold.

6. The method of claim 5, wherein the second frequency range is lower than the first frequency range and separated from the first frequency range by a third frequency range, and also including the steps of:

determining whether the data signal's bit rate is in the first frequency range, the second frequency range, or the third frequency range;

after application of the first low-pass filter has begun, continuing to apply the first low-pass filter in response to determining that the data signal's bit rate has decreased from a value in the first frequency range to a value in the third frequency range but above the second frequency range; and

after application of the first low-pass filter has ceased, recommencing application of the first low-pass filter only in response to determining that the data signal's bit rate has increased from a value below the first frequency range to a value in the first frequency range.

7. The method of claim 1, also including the step of:

selecting those of the samples that were generated at the sequence of best sampling positions identified in step (b).

8. A method for selecting samples of a data signal having a data eye, where the data eye has a center and the samples have been generated by oversampling the data signal using an oversampling clock, said method including the steps of:

(a) generating sampling position control data in response to relative phase data, where the relative phase data are indicative of the phase of a selected sampling position of the oversampling clock relative to the center of the data eye during at least one tracking period of said data signal;

(b) generating additional relative phase data such that the additional relative phase data are indicative of the phase of each of multiple sampling positions of the oversampling clock relative to the center of the data eye during a subsequent tracking period of the data signal;

(c) after step (b), selecting a subset of a set of the samples and a subset of the additional relative phase data in response to the sampling position control data, wherein the set of the samples has been generated by oversampling the data signal during the subsequent tracking period, the subset of the set of the samples has been generated at the selected sampling position, and the subset of the additional relative phase data is indicative of the phase of the selected sampling position relative to the center of the data eye during the subsequent tracking period; and

(d) after step (c), generating updated sampling position control data in response to the subset of the additional relative phase data selected during step (c).

9. The method of claim 8, wherein the relative phase data employed in step (a) are indicative of the phase of the selected sampling position of the oversampling clock relative to the center of the data eye during each of at least two consecutive tracking periods of said data signal.

10. The method of claim 9, wherein the subset of the additional relative phase data employed in step (d) is indicative of the phase of the selected sampling position of the oversampling clock relative to the center of the data eye during each of at least two consecutive tracking periods of said data signal including the subsequent tracking period.

11. A method for selecting samples of a data signal having a data eye, where the data eye has a center and the samples have been generated by oversampling the data signal using an oversampling clock, said method including the steps of:

(a) generating sampling position control data in response to relative phase data, where the relative phase data are indicative of the phase of a selected sampling position of the oversampling clock relative to the center of the data eye during at least one tracking period of said data signal;

(b) generating additional relative phase data, wherein the additional relative phase data are indicative of the phase of each of multiple sampling positions of the oversampling clock relative to the center of the data eye during a subsequent tracking period of said data signal;

(c) after step (b), selecting a subset of a set of the samples and a subset of the additional relative phase data in response to the sampling position control data, wherein the set of the samples has been generated by oversampling the data signal during one tracking period of said at least one tracking period, the subset of the set of the samples has been generated at the selected sampling position, and the subset of the additional relative phase data is indicative of the phase of the selected sampling position relative to the center of the data eye during the subsequent tracking period; and

(d) after step (c), generating updated sampling position control data in response to the subset of the additional relative phase data selected during step (c).

12. The method of claim 11, wherein the relative phase data employed in step (a) are indicative of the phase of the selected sampling position of the oversampling

clock relative to the center of the data eye during each of at least two consecutive tracking periods of said data signal.

13. The method of claim 12, wherein the subset of the additional relative phase data employed in step (d) is indicative of the phase of the selected sampling position of the oversampling clock relative to the center of the data eye during each of at least two consecutive tracking periods of said data signal including the subsequent tracking period.

14. A method for identifying a sequence of selected sampling positions for sampling a data signal by processing a sequence of sample sets, where each of the sample sets consists of samples of the data signal that have been generated by oversampling said data signal during a different tracking period, said method including the steps of:

(a) for each of the sample sets, determining whether said each of the sample sets indicates that the data signal has less than a predetermined number of transitions during the tracking period in which said each of the sample sets was generated; and

(b) identifying the sequence of selected sampling positions by processing the sequence of sample sets, including by selecting a different sampling position to replace a previously selected sampling position only in response to each of the sample sets that indicates that the data signal has at least the predetermined number of transitions during the tracking period in which said each of the sample sets was generated, but not in response to any of the sample sets that indicates that the data signal has less than the predetermined number of transitions during the tracking period in which said any one of the sample sets was generated.

15. The method of claim 14, wherein each of the sample sets consists of samples of the data signal that have been generated by oversampling said data signal using an oversampling clock having sampling positions, and wherein step (b) includes the steps of:

generating, from the sample sets, relative phase data indicative of the phase of each of at least one of the sampling positions of the oversampling clock relative to the center of the data eye, for each of at least two tracking periods of the data signal; and

determining from the relative phase data which of the sampling positions is best aligned with the center of the data eye during each of at least some of the tracking periods, thereby identifying the sequence of selected sampling positions.

16. The method of claim 14, also including the step of:

selecting those of the samples that were generated at the sequence of selected sampling positions identified in step (b).

17. A phase tracker for receiving samples of a data signal having a variable bit rate, said samples having been generated by oversampling the data signal at each of at least two sampling positions, said phase tracker including:

sampling position control circuitry configured to generate, in response to the samples, sampling position control data indicative of a selected one of the sampling positions for each of a sequence of tracking periods of the data signal; and

frequency zone detection logic configured to generate a frequency range signal indicative of a frequency range that contains the data signal's bit rate,

wherein the sampling position control circuitry includes low-pass filter circuitry coupled to receive the frequency range signal and configured to operate in a first mode when the frequency range signal indicates that the bit rate exceeds a first threshold frequency, wherein the low-pass filter circuitry generates filtered data in the first mode, and the sampling position control circuitry is configured to generate the sampling position control data in response to the filtered data when the low-pass filter circuitry operates in the first mode.

18. The phase tracker of claim 17, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode generates differently filtered data, and the sampling position control circuitry is configured to generate the sampling position control data in response to the differently filtered data when the low-pass filter circuitry operates in the second mode.

19. The phase tracker of claim 17, wherein the sampling position control circuitry is configured to disable or bypass the low-pass filter circuitry during

generation of the sampling position control data when the frequency range signal indicates that the bit rate is less than a second threshold frequency.

20. A phase tracker configured to receive samples of a data signal having a data eye and a variable bit rate, said samples having been generated by oversampling the data signal at each of at least two sampling positions, where the data eye has a center, said phase tracker including:

sampling position control data generation circuitry configured to generate relative phase data in response to the samples, and to generate intermediate data and sampling position control data in response to the relative phase data, wherein the relative phase data are indicative of the phase of each of the sampling positions relative to the center of the data eye for each of at least two tracking periods of the data signal, and the sampling position control data are indicative of which of the sampling positions is best aligned with the center of the data eye during each of the tracking periods; and

frequency zone detection logic configured to generate a frequency range signal indicative of a frequency range that contains the data signal's bit rate,

wherein the sampling position control data generation circuitry includes low-pass filter circuitry coupled to receive the frequency range signal and configured to operate in a first mode when the frequency range signal indicates that the bit rate exceeds a first threshold frequency, wherein the low-pass filter circuitry in the first mode applies a first low pass filter to the intermediate data, thereby generating filtered data, and the sampling position control data generation circuitry is configured to generate the sampling position control data in response to the filtered data when the low-pass filter circuitry operates in the first mode.

21. The phase tracker of claim 20, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode applies a second low pass filter to the intermediate data, thereby generating differently filtered data, and the sampling position control data generation circuitry is configured to generate the sampling position control data in response to the differently filtered data when the low-pass filter circuitry operates in the second mode.

22. The phase tracker of claim 21, wherein the low-pass filter circuitry has a selectable number of taps, and fewer of the taps are selected when the low-pass filter circuitry operates in the second mode than when the low-pass filter circuitry operates in the first mode.

23. The phase tracker of claim 22, wherein the second threshold frequency is lower than the first threshold frequency.

24. The phase tracker of claim 20, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode does not low-pass filter the intermediate data, and the sampling position control data generation circuitry is configured to generate the sampling position control data in response to the intermediate data when the low-pass filter circuitry operates in the second mode.

25. The phase tracker of claim 24, wherein the second threshold frequency is lower than the first threshold frequency.

26. The phase tracker of claim 20, wherein the frequency zone detection logic is configured to generate the frequency range signal so that the frequency range signal exhibits hysteresis.

27. The phase tracker of claim 20, wherein the frequency zone detection logic is configured to generate the frequency range signal so that the frequency range signal has a first value when the bit rate is in a first frequency range and a second value when the bit rate is in a second frequency range, the second frequency range is lower than the first frequency range and separated from the first frequency range by a third frequency range, the frequency zone detection logic is configured to generate the frequency range signal so as to have the first value in response to determining that the bit rate has decreased from a value in the first frequency range to a value in the third frequency range but above the second frequency range, and the frequency zone detection logic is configured to generate the frequency range signal so as to have the second value in

response to determining that the bit rate has increased from a value in the second frequency range to a value in the third frequency range.

28. The phase tracker of claim 20, wherein the frequency zone detection logic includes:

a counter configured to generate a count indicative of the number of cycles of a data clock that occur during a predetermined number of cycles of a second clock having a fixed, predetermined frequency, where the data clock has frequency indicative of the data signal's bit; and

logic coupled to the counter and configured to generate the frequency range signal in response to the count.

29. A circuit for oversampling a data signal having a data eye and a variable bit rate, where the data eye has a center, said circuit including:

sampling circuitry configured to oversample the data signal, thereby generating samples of the data signal at each of at least two sampling positions;

a phase tracker coupled and configured to generate relative phase data in response to the samples and to generate intermediate data and sampling position control data in response to the relative phase data, wherein the relative phase data are indicative of the phase of each of the sampling positions relative to the center of the data eye for each of at least two tracking periods of the data signal, and the sampling position control data are indicative of which of the sampling positions is best aligned with the center of the data eye during each of the tracking periods; and

sample selection circuitry coupled and configured to select a subset of the samples for each of the tracking periods in response to the sampling position control data,

wherein the phase tracker includes:

frequency zone detection logic configured to generate a frequency range signal indicative of a frequency range that contains the data signal's bit rate; and

low-pass filter circuitry coupled to receive the frequency range signal and configured to operate in a first mode when the frequency range signal indicates that the bit rate exceeds a first threshold frequency, wherein the low-pass filter circuitry in the first mode applies a first low pass filter to the intermediate data, thereby generating filtered data, and the phase tracker is configured to generate the sampling position

control data in response to the filtered data when the low-pass filter circuitry operates in the first mode.

30. The circuit of claim 29, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode applies a second low pass filter to the intermediate data, thereby generating differently filtered data, and the phase tracker is configured to generate the sampling position control data in response to the differently filtered data when the low-pass filter circuitry operates in the second mode.

31. The circuit of claim 30, wherein the low-pass filter circuitry has a selectable number of taps, and fewer of the taps are selected when the low-pass filter circuitry operates in the second mode than when the low-pass filter circuitry operates in the first mode.

32. The circuit of claim 31, wherein the second threshold frequency is lower than the first threshold frequency.

33. The circuit of claim 29, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode does not low-pass filter the intermediate data, and the phase tracker is configured to generate the sampling position control data in response to the intermediate data when the low-pass filter circuitry operates in the second mode.

34. The circuit of claim 33, wherein the second threshold frequency is lower than the first threshold frequency.

35. The circuit of claim 29, wherein the frequency zone detection logic is configured to generate the frequency range signal so that the frequency range signal exhibits hysteresis.

36. The circuit of claim 29, wherein the frequency zone detection logic is configured to generate the frequency range signal so that the frequency range signal has a first value when the bit rate is in a first frequency range and a second value when the bit rate is in a second frequency range, the second frequency range is lower than the first frequency range and separated from the first frequency range by a third frequency range, the frequency zone detection logic is configured to generate the frequency range signal so as to have the first value in response to determining that the bit rate has decreased from a value in the first frequency range to a value in the third frequency range but above the second frequency range, and the frequency zone detection logic is configured to generate the frequency range signal so as to have the second value in response to determining that the bit rate has increased from a value in the second frequency range to a value in the third frequency range.

37. The circuit of claim 29, wherein the frequency zone detection logic includes:

a counter configured to generate a count indicative of the number of cycles of a data clock that occur during a predetermined number of cycles of a second clock having a fixed, predetermined frequency, where the data clock has frequency indicative of the data signal's bit; and

logic coupled to the counter and configured to generate the frequency range signal in response to the count.

38. A circuit for oversampling a data signal having a data eye, where the data eye has a center, said circuit including:

sampling circuitry configured to oversample the data signal using an oversampling clock having multiple sampling positions, thereby generating samples of the data signal at each of the sampling positions; and

a pipelined phase tracker coupled and configured to generate relative phase data in response to the samples and to generate sampling position control data in response to the relative phase data, wherein the phase tracker includes:

first circuitry coupled and configured to receive those of the samples generated during a tracking period of the data signal and to generate a first quantity of the relative phase data in response to the received samples, wherein the first quantity of the relative

phase data is indicative of the phase of each the sampling positions relative to the center of the data eye during the tracking period;

second circuitry coupled to receive the first quantity of the relative phase data, a set of the samples, and a first quantity of the sampling position control data generated in response to a second quantity of the relative phase data indicative of the phase of at least one the sampling positions relative to the center of the data eye during at least one other tracking period of the data signal, wherein the second circuitry is configured to select a subset of the first quantity of the relative phase data and a subset of the set of the samples in response to the first quantity of the sampling position control data, such that the subset of the first quantity of the relative phase data is indicative of the phase of a selected one of the sampling positions relative to the center of the data eye, and such that the subset of the set of the samples was generated at the selected one of the sampling positions; and

third circuitry, coupled to receive the subset of the first quantity of the relative phase data and configured to generate a second quantity of the sampling position control data in response thereto.

39. The circuit of claim 38, wherein the set of the samples received by the second circuitry are the samples generated during the tracking period, and the subset of said set of the samples was generated at the selected one of the sampling positions during said tracking period.

40. The circuit of claim 38, wherein the second quantity of the relative phase data is indicative of the phase of one the sampling positions relative to the center of the data eye during each of at least two previous tracking periods of said data signal.

41. A pipelined phase tracker configured to receive samples of a data signal having a data eye, where the data eye has a center and the samples have been generated by oversampling the data signal at each of at least two sampling positions, said phase tracker including:

first circuitry configured to receive those of the samples generated during a tracking period of the data signal and to generate a first quantity of relative phase data in response to said samples, wherein the first quantity of relative phase data is

indicative of the phase of each the sampling positions relative to the center of the data eye during the tracking period;

second circuitry coupled to receive the first quantity of relative phase data, a set of the samples, and a first quantity of sampling position control data generated in response to a second quantity of relative phase data, wherein the second quantity of relative phase data is indicative of the phase of at least one the sampling positions relative to the center of the data eye during at least one other tracking period, and the second circuitry is configured to select a subset of the first quantity of relative phase data and a subset of the set of the samples in response to the first quantity of sampling position control data, such that the subset of the first quantity of relative phase data is indicative of the phase of a selected one of the sampling positions relative to the center of the data eye, and such that the subset of the set of the samples was generated at the selected one of the sampling positions; and

third circuitry, coupled to receive the subset of the first quantity of relative phase data and configured to generate a second quantity of sampling position control data in response thereto.

42. The phase tracker of claim 41, wherein the set of the samples received by the second circuitry are the samples generated during the tracking period, and the subset of said set of the samples was generated at the selected one of the sampling positions during said tracking period.

43. The phase tracker of claim 41, wherein the second quantity of relative phase data is indicative of the phase of one the sampling positions relative to the center of the data eye during each of at least two previous tracking periods of said data signal.

44. A circuit for oversampling a data signal, said circuit including:

sampling circuitry configured to oversample the data signal using an oversampling clock having multiple sampling positions, thereby generating samples of the data signal at each of the sampling positions during each tracking period of a sequence of tracking periods; and

a phase tracker coupled and configured to receive a sequence of sample sets and to determine a sequence of selected sampling positions for sampling the data signal in response to the sample sets, wherein each of the sample sets is a set of the samples

generated during a different one of the tracking periods and each of the selected sampling positions is for a different one of the tracking periods, wherein the phase tracker includes:

logic circuitry coupled and configured to generate transition data in response to the sample sets, wherein the transition data include transition data for each of the tracking periods indicating whether the data signal has less than a predetermined number of transitions during said each of the tracking periods; and

additional logic circuitry coupled and configured to determine the sequence of selected sampling positions in response to the transition data and the sample sets, including by selecting an updated sampling position to replace a previously selected sampling position only in response to each of the sample sets for which the transition data indicate that the data signal has at least the predetermined number of transitions during the tracking period in which said each of the sample sets was generated, but not in response to any of the sample sets for which the transition data indicate that the data signal has less than the predetermined number of transitions during the tracking period in which said any of the sample sets was generated.

45. The circuit of claim 44, wherein the data signal has a data eye, the data eye has a center, and the additional logic includes:

logic configured to generate, from the sample sets, relative phase data indicative of the phase of each of at least one of the sampling positions of the oversampling clock relative to the center of the data eye, for each of at least two of the tracking periods of the data signal; and

logic configured to determine from the relative phase data which of the sampling positions is best aligned with the center of the data eye during each of at least some of the tracking periods.

46. A phase tracker configured to receive a sequence of sample sets, wherein each of the sample sets is a subset of a sequence of samples of a data signal, the samples in the sequence have been generated using an oversampling clock having multiple sampling positions and include samples of the data signal at each of the sampling positions during each tracking period of a sequence of tracking periods, and each of the sample sets consists of samples generated during a different one of the tracking periods, said phase tracker including:

logic circuitry configured to generate transition data in response to the sample sets, wherein the transition data include transition data for each of the tracking periods indicating whether the data signal has less than a predetermined number of transitions during said each of the tracking periods; and

additional logic circuitry coupled and configured to determine a sequence of selected sampling positions for sampling the data signal in response to the transition data and the sample sets, including by selecting an updated sampling position to replace a previously selected sampling position only in response to each of the sample sets for which the transition data indicate that the data signal has at least the predetermined number of transitions during the tracking period in which said each of the sample sets was generated, but not in response to any of the sample sets for which the transition data indicate that the data signal has less than the predetermined number of transitions during the tracking period in which said any of the sample sets was generated, wherein each of the selected sampling positions is for a different one of the tracking periods.

47. The circuit of claim 46, wherein the data signal has a data eye, the data eye has a center, and the additional logic includes:

logic configured to generate, from the sample sets, relative phase data indicative of the phase of each of at least one of the sampling positions of the oversampling clock relative to the center of the data eye, for each of at least two of the tracking periods of the data signal; and

logic configured to determine from the relative phase data which of the sampling positions is best aligned with the center of the data eye during each of at least some of the tracking periods.

48. A receiver configured to receive at least one data signal that has been transmitted over a serial link, said data signal having a data eye and a variable bit rate, where the data eye has a center, said receiver including:

sampling circuitry configured to oversample the data signal; and

a phase tracker coupled to receive samples of the data signal from the sampling circuitry, said samples having been generated by oversampling said data signal at each of at least two sampling positions, wherein the phase tracker includes:

sampling position control data generation circuitry coupled and configured to generate relative phase data in response to the samples, and to generate intermediate

data and sampling position control data in response to the relative phase data, wherein the relative phase data are indicative of the phase of each of the sampling positions relative to the center of the data eye for each of at least two tracking periods of the data signal, and the sampling position control data are indicative of which of the sampling positions is best aligned with the center of the data eye during each of the tracking periods; and

frequency zone detection logic configured to generate a frequency range signal indicative of a frequency range that contains the data signal's bit rate,

wherein the sampling position control data generation circuitry includes low-pass filter circuitry coupled to receive the frequency range signal and configured to operate in a first mode when the frequency range signal indicates that the bit rate exceeds a first threshold frequency, wherein the low-pass filter circuitry in the first mode applies a first low pass filter to the intermediate data, thereby generating filtered data, and the sampling position control data generation circuitry is configured to generate the sampling position control data in response to the filtered data when the low-pass filter circuitry operates in the first mode.

49. The receiver claim 48, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode applies a second low pass filter to the intermediate data, thereby generating differently filtered data, and the sampling position control data generation circuitry is configured to generate the sampling position control data in response to the differently filtered data when the low-pass filter circuitry operates in the second mode.

50. The receiver of claim 48, wherein the low-pass filter circuitry is configured to operate in a second mode when the frequency range signal indicates that the bit rate is less than a second threshold frequency, the low-pass filter circuitry in the second mode does not low-pass filter the intermediate data, and the sampling position control data generation circuitry is configured to generate the sampling position control data in response to the intermediate data when the low-pass filter circuitry operates in the second mode.

51. The receiver of claim 50, wherein the second threshold frequency is lower than the first threshold frequency.

52. A receiver configured to receive at least one data signal that has been transmitted over a serial link, said data signal having a data eye, where the data eye has a center, said receiver including:

sampling circuitry configured to oversample the data signal; and

a pipelined phase tracker coupled to receive samples of the data signal from the sampling circuitry, said samples having been generated by oversampling said data signal at each of at least two sampling positions, wherein the phase tracker includes:

first circuitry coupled and configured to receive those of the samples generated during a tracking period of the data signal and to generate a first quantity of relative phase data in response to said samples, wherein the first quantity of relative phase data is indicative of the phase of each the sampling positions relative to the center of the data eye during the tracking period;

second circuitry coupled to receive the first quantity of relative phase data, a set of the samples, and a first quantity of sampling position control data generated in response to a second quantity of relative phase data, wherein the second quantity of relative phase data is indicative of the phase of at least one the sampling positions relative to the center of the data eye during at least one other tracking period, and the second circuitry is configured to select a subset of the first quantity of relative phase data and a subset of the set of the samples in response to the first quantity of sampling position control data, such that the subset of the first quantity of relative phase data is indicative of the phase of a selected one of the sampling positions relative to the center of the data eye, and such that the subset of the set of the samples was generated at the selected one of the sampling positions; and

third circuitry, coupled to receive the subset of the first quantity of relative phase data and configured to generate a second quantity of sampling position control data in response thereto.

53. The receiver of claim 52, wherein the set of the samples received by the second circuitry are the samples generated during the tracking period, and the subset of said set of the samples was generated at the selected one of the sampling positions during said tracking period.

54. A receiver configured to receive at least one data signal that has been transmitted over a serial link, said data signal having a data eye, where the data eye has a center, said receiver including:

sampling circuitry configured to generate a sequence of samples of the data signal using an oversampling clock having multiple sampling positions, so that the samples in the sequence include samples of the data signal at each of the sampling positions during each tracking period of a sequence of tracking periods; and

a phase tracker coupled to receive a sequence of sample sets, wherein each of the sample sets is a subset of the sequence of samples of the data signal, each of the sample sets consists of samples generated during a different one of the tracking periods, and the phase tracker includes:

logic circuitry coupled and configured to generate transition data in response to the sample sets, wherein the transition data include transition data for each of the tracking periods indicating whether the data signal has less than a predetermined number of transitions during said each of the tracking periods; and

additional logic circuitry coupled and configured to determine a sequence of selected sampling positions for sampling the data signal in response to the transition data and the sample sets, including by selecting an updated sampling position to replace a previously selected sampling position only in response to each of the sample sets for which the transition data indicate that the data signal has at least the predetermined number of transitions during the tracking period in which said each of the sample sets was generated, but not in response to any of the sample sets for which the transition data indicate that the data signal has less than the predetermined number of transitions during the tracking period in which said any of the sample sets was generated, wherein each of the selected sampling positions is for a different one of the tracking periods.